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EXAMINER	
DANG, KHANH	
ART UNIT	PAPER NUMBER
2111	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/626,756	TRAYNOR ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 7-20 and 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 7-13 are directed to an apparatus. However, the essential structural cooperative relationship(s) between the so-called "logic that maps," "logic that selectively enables," "logic that determines," "logic that advances," "logic that sets," "logic that dynamically modifies," and "logic that defines" have been omitted, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

Claims 14-20 are directed to an apparatus. However, the essential structural cooperative relationship(s) between the so-called "plurality of logical ANDs" and "logical OR" have been omitted, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

Claim 23 is also directed to an apparatus. However, the essential structural cooperative relationship(s) between the so-called "logic that maps" and "logic that selectively enables" have been omitted, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

MPEP 2172.01 requires that relationships between elements recited in the claims must be specified. Specifically, MPEP 2172.02 requires interrelation and structural relationships between essential elements in the claims. Therefore, it is the Examiner's

position that the claimed elements, as defined in the originally filed specification and as identified above, are essential elements to the claimed invention. Since they are essential elements as defined in the originally filed specification, their structural cooperative relationships must be provided in the claims. Further, it is also the Examiner's position that the claimed elements, as identified above, function simultaneously, are directly functionally related, directly inter-cooperate, and/or serve independent purposes, as evidenced from the originally filed specification.

If Applicants disagree with the Examiner that the above identified elements, as defined by the originally filed specification, are essential elements to the claimed invention, and that the above identified elements are directly functionally related, directly inter-cooperate, and/or serve independent purposes, it is requested that Applicants provide evidences showing that the identified elements are not essential elements to the claimed invention, do not function simultaneously, are not directly functionally related, do not directly inter-cooperate, and/or do not serve independent purposes; and state for the record that this is the case.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent

granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 7, new claim 21, and new claim 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Armstrong (5,764,996).

As broadly drafted, claims 1, 7, 21, and 23 do not define any structure/step that differs from Armstrong. As a matter of fact, by drafting claims 1, 7, 21, and 23, Applicants are attempting to claim the notoriously well-known interrupt sharing architecture defined by the PCI Local Bus Specification, as described in Fig. 2 of Armstrong, and specifically disclosed in column 1, lines 37-43 and column 2, lines 56-67.

With regard to 1, Armstrong discloses that method for sharing a plurality of interrupt inputs associated with a processor among a plurality of interrupt sources, comprising the steps of: mapping each of the plurality of interrupt sources to each of the plurality of interrupt inputs; and selectively enabling interrupt requests from each of the plurality of interrupt sources to one or more of the plurality of interrupt inputs (Armstrong discloses that, according to the PCI Local Bus Specification adopts a shared or wired-OR interrupt binding architecture. As shown in Fig. 2:

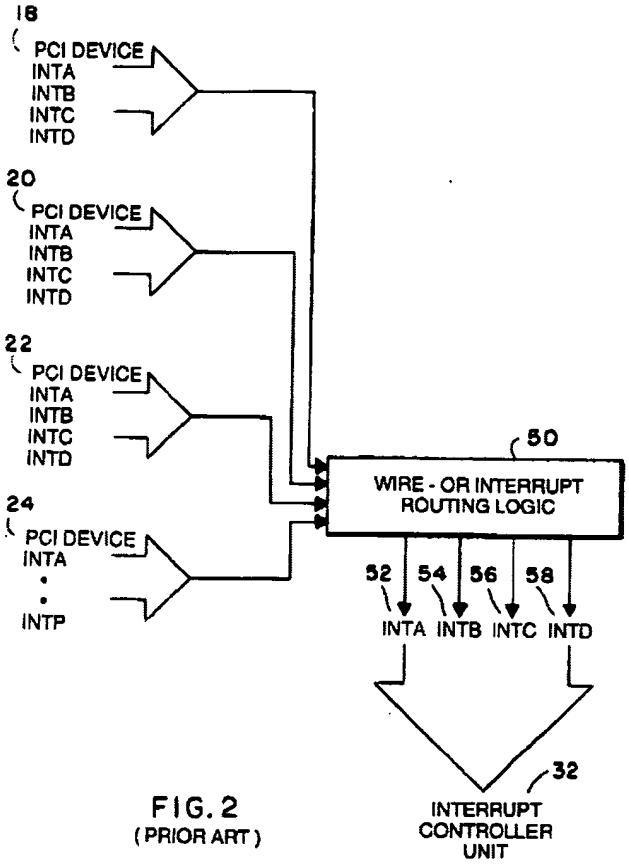

FIG. 2
(PRIOR ART)

all PCI interrupt sources are wired-OR'ed in the wired-OR interrupt routing logic 50 to map into interrupt inputs INTA – INTD of the interrupt controller 32. As well-defined in computer architecture, the logic OR gate selectively enable an output based on values of the 2 inputs:

OR gate

Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	1

Thus, it is clear that the wired-OR serves as a decision making unit to selectively enable PCI interrupt requests from each of the plurality of PCI interrupt sources to one or more of the plurality of interrupt inputs INTA – INTD of the interrupt controller 32.

With regard to claims 7, 21, and 23, see discussion above, since the subject matter presented in these claims has already been addressed.

Claims 1-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Wach (5,530,875).

With regard to claim 1, Wach discloses a method for sharing a plurality of interrupt inputs associated with a processor among a plurality of interrupt sources, comprising the steps of: mapping each of the plurality of interrupt sources to each of the plurality of interrupt inputs; and selectively enabling interrupt requests from each of the plurality of interrupt sources to one or more of the plurality of interrupt inputs (Wach

discloses an interrupt architecture employing interrupt sharing, which is best illustrated in the following figure:

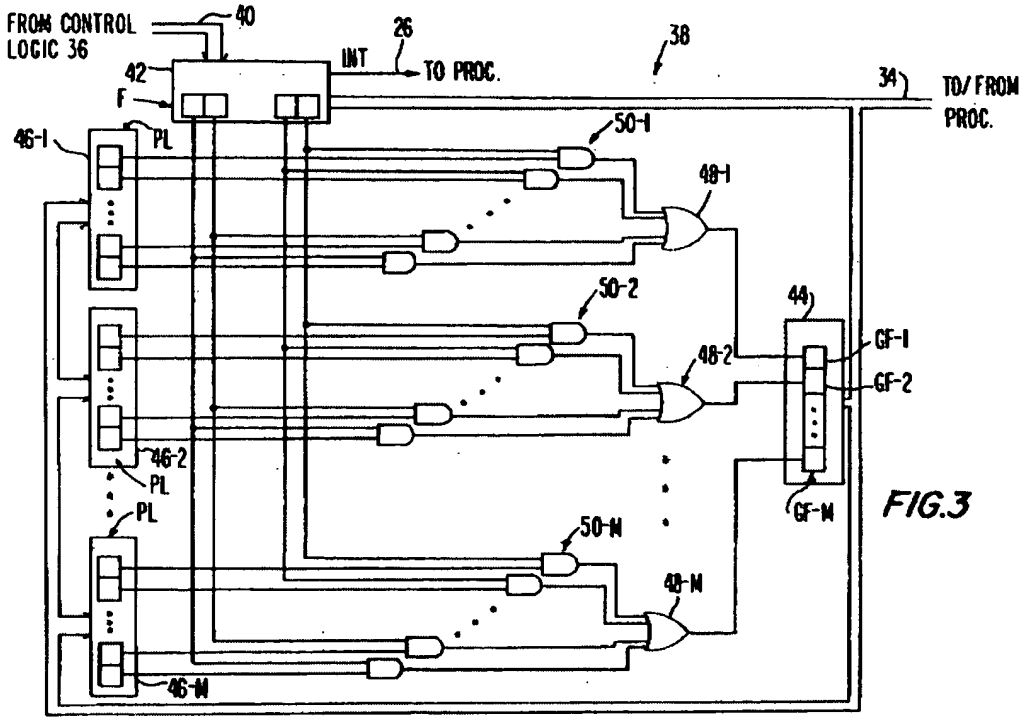

FIG.3

At the outset, in order to have a clear understanding of the following discussion, it is important to note that the interrupt requests can be generated from register 44 instead of register 42 (see column 11, lines 10-15). In addition, the term "group" used in Wash includes group that has only one interrupt resource (see column 11, lines 47-49).

As shown above and specifically described in column 4, line 63 to column 6, line 43; column 10, line 55 to column 11, line 48, the number of storage locations F in register 42 is equal to the number of interrupt sources, any one of which may cause the

transmission of the interrupt signal to processor 14. Also, the locations F correspond one-to-one to the interrupt sources. The plurality of interrupt resources are routed or mapped to a plurality of interrupt inputs represented by a plurality of locations GF; wherein the interrupt request signal generated when any one or more of the locations GF are set. Further, in Wash, a masking bit is used to enable or disable interrupt requests from each of a plurality of interrupt sources to one or more of the plurality of interrupt inputs. Specifically, when it is desired to mask a given one of the interrupt sources, processor 14 sends programming signals to the association registers 46 such that the value "0" is stored in the respective location PL corresponding to the interrupt source to be masked.

With regard to claim 2, as discussed above, when it is desired to mask a given one of the interrupt sources, processor 14 sends programming signals to the association registers 46 such that the value "0" is stored in the respective location PL corresponding to the interrupt source to be masked.

With regard to claim 3, as discussed above, when it is desired to mask a given one of the interrupt sources, processor 14 sends programming signals to the association registers 46 such that the value "0" is stored in the respective location PL corresponding to the interrupt source to be masked. Further, as also discussed above, each location PL corresponds to each of interrupt source. Thus, it is clear that a control bit value can be selectively set in each of location PL corresponding to the mapped interrupt source/interrupt input combination.

With regard to claim 4, as discussed above, the masking control bit is programmable. Thus, it is clear that the control bit values can be set according to user preferences.

With regard to claim 5, as discussed above, the masking control bit is programmable. Thus, it is clear that the control bit values can be dynamically modified according to user preferences.

With regard to claim 6, it is clear that the control bit values must be defined according to system requirements. Further, it is also clear that the system of Wash comprises the processor, at least one interrupt source, and at least one interrupt input.

With regard to claims 7-12, see discussion above, since the subject matter presented in claims 7-12 has already been addressed.

With regard to claim 13, as clearly shown in the figure above, the logic that selectively enables comprises, for each mapped interrupt source/interrupt input combination, a logical AND (50) for ANDing each interrupt source with a respective control bit value.

With regard to claim 14, Wash discloses a system for sharing a plurality of interrupt inputs associated with a processor among a plurality of interrupt sources (Wach discloses an interrupt architecture employing interrupt sharing, which is best illustrated in the following figure:

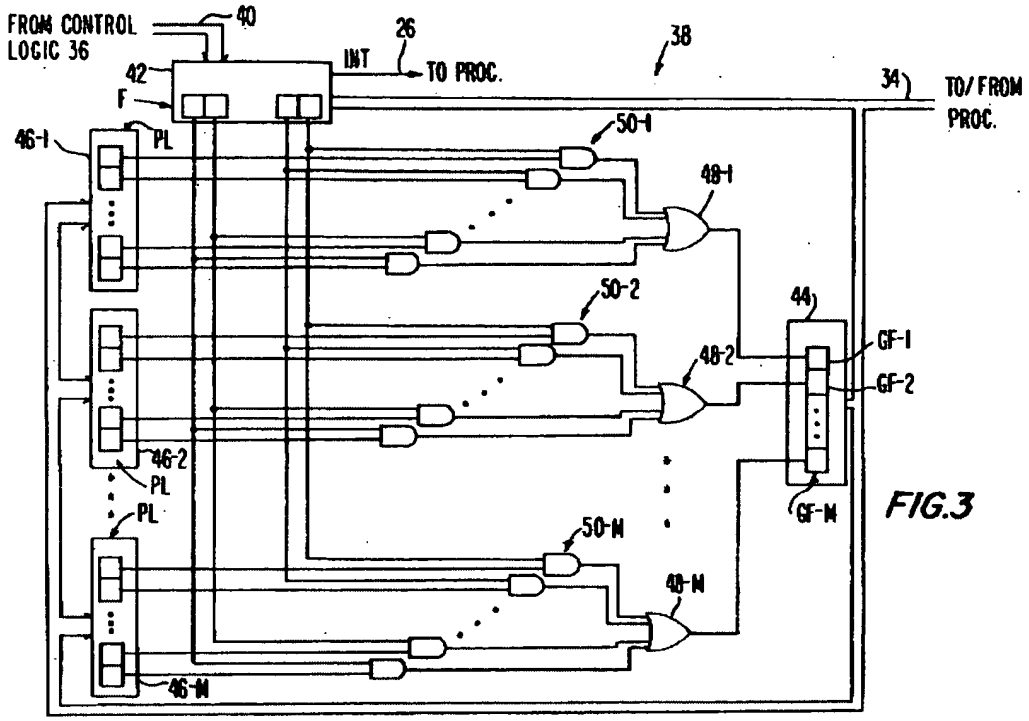

FIG.3

, comprising: for each of said plurality of interrupt inputs: a plurality of logical ANDs, each corresponding to an interrupt source, the corresponding interrupt source providing an interrupt request signal to the corresponding logical AND to interrupt the processor (a plurality of AND gates 50, each having an input to receive an interrupt request signal from an interrupt source to interrupt the processor; see also discussion above regarding claim 1); a plurality of control bits each corresponding to an interrupt source and each respectively providing a control bit value to the corresponding logical AND (a plurality of masking bits, each can be set in the location PL to provide a control value to the other input of AND gate 50; see also discussion regarding claim 1 above), wherein, based on the control bit value, a corresponding interrupt request signal is

provided at an output of the corresponding logical AND (based on the control bit value provided at one input of the AND gate, an interrupt request signal is provided at output of the AND gate 50; see also discussion above regarding claim 1); a logical OR arranged to indicate, to the interrupt input, the presence of a corresponding interrupt request signal from at least one output of the plurality of logical ANDs (as clearly discussed above regarding claim 1, the OR gate 48 is arranged to indicate the presence of a corresponding interrupt request signal from at least one output of the plurality of AND gates 50 to the interrupt input; see also discussion above regarding claim 1).

With regard to claims 15-20, see discussion above, since the subject matter presented in claims 15-20 has already been addressed.

Response to Arguments

Applicants' arguments filed 2/13/2007 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997).* As a matter of fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.,* 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification

cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

The 112 Rejection:

With regard to the 112 Rejection, Applicants argued that "MPEP £32172.01 entitled, 'Unclaimed Essential Matter', discusses claims which omit matter disclosed to be essential to the invention as described in the specification or in other statements of record. However, the Office Action does not indicate portions of the specification or other statements in the record where the Applicants specifically state that the structural connections are necessary to practice the claimed invention, or define interrelationships between essential elements of the invention. Applicants' description of Figures 3 and 4 (see page 5, paragraphs [0016] and [0017], page 6, paragraph [0022], and page 8, paragraph [0027] of Applicants' specification) refer to a system and method for interrupt mapping according to an aspect of the invention. The phrase 'according to an aspect of the invention' indicates that the illustrations provided in the figures are exemplary, and that one of skill in the art may be able to derive a circuit or flow diagram, different from those illustrated in the figures, that comprise the claimed logic and method steps. Therefore, Applicants respectfully submit that specific structural connections, beyond

those recited in the present claims, are not necessary to point out the subject matter that applicants regard as their invention. Based on the above, the Applicants assert that the claims comply with the requirements of 35 U.S.C. §112, and request withdrawal of the rejection of claims 7-20 and 23 under this section of the statute."

In response to Applicants' argument, at the outset, it is noted that 35 USC 112, 1st paragraph requires that:

> "The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention."

As cited by Applicants, the "Applicants' description of Figures 3 and 4 (see page 5, paragraphs [0016] and [0017], page 6, paragraph [0022], and page 8, paragraph [0027] of Applicants' specification) refer to a system and method for interrupt mapping according to an aspect of the invention." Whether there may be other aspects, Figures, diagrams that are not disclosed in the specification and the claims are irrelevant under consideration of 35 USC 112, 1st and 2nd paragraphs. As disclosed by the relevant disclosure, cited by Applicants, it is clear that the structures set forth in claims 7-20 and 23 are essential to the invention. The Examiner also maintains his position that the interrupt mapping structures, as disclosed by the originally filed specification, are

essential to the claimed invention. If Applicants disagree with the Examiner that the above identified elements, as defined by the originally filed specification, are essential elements to the claimed invention, and that the above identified elements are directly functionally related, directly inter-cooperate, and/or serve independent purposes, it is requested that Applicants provide evidences showing that the identified elements are not essential elements to the claimed invention, do not function simultaneously, are not directly functionally related, do not directly inter-cooperate, and/or do not serve independent purposes; and state for the record that this is the case.

To assist Applicants, it is advised that the claims should be amended to incorporate terms such as "connected" or operatively connected" to provide structural connections between elements in the claims.

The Armstrong 102 Rejection:

With regard to claims 1, 7, 21-23, Applicants argued that "[s]ince the claimed interrupt sources of the reference have not been identified in the Office Action, Applicants assume that INTA, INTB, INTC and INTD of each PCI device, 18, 20, 22 and 24 of the Armstrong patent, are being interpreted as the interrupt sources. In addition, the Applicants understand the Office Action to be interpreting INTA 52, INTB 54, INTC 56 and INTD 58 as the interrupt inputs. The description of Figure 2 of the Armstrong patent does not indicate that each INTA, INTB, INTC and INTD of each PCI device 18, 20, 22 and 24 is mapped to each interrupt input. For instance, there is no disclosure that INTA of PCI device 18 is mapped to INTB 54, INTC 56 and INTD 58.

Applicants respectfully submit that each of the plurality of interrupt sources is not mapped to each of the plurality of interrupt inputs, as recited in the independent claims. Rather, each interrupt source is only mapped to one interrupt input. As such, the Armstrong patent is representative of the prior art illustrated in Figure 1 of the present application. "

In response to Applicants' argument, at the outset, a relevant portion of the Armstrong 102 Rejection is reproduced below:

Armstrong discloses that, according to the PCI Local Bus Specification adopts a shared or wired-OR interrupt binding architecture. As shown in Fig. 2:

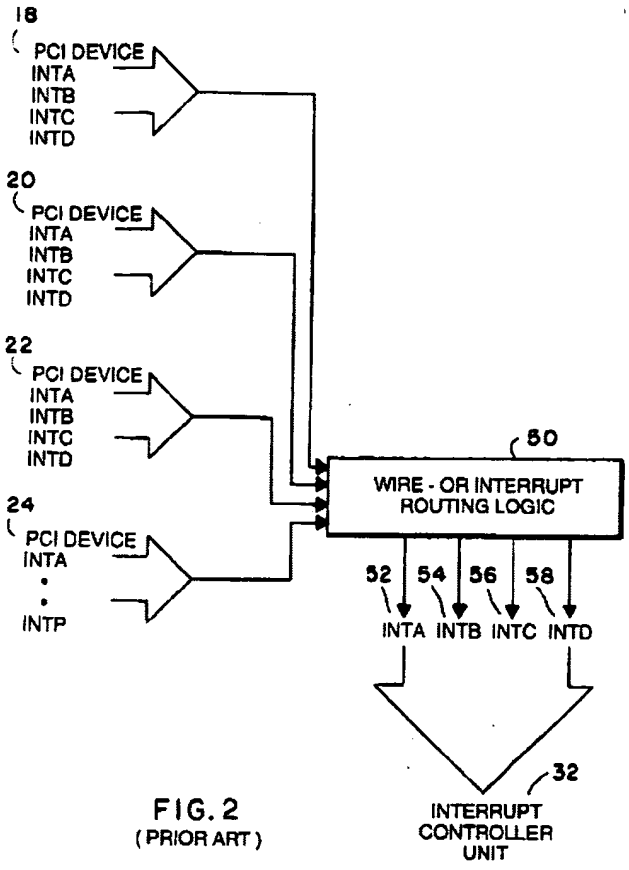

FIG. 2
(PRIOR ART)

all PCI interrupt sources are wired-OR'ed in the wired-OR interrupt routing logic 50 to map into interrupt inputs INTA – INTD of the interrupt controller 32. As well-defined in computer architecture, the logic OR gate selectively enable an output based on values of the 2 inputs:

OR gate

Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	1

Thus, it is clear that the wired-OR serves as a decision making unit to selectively enable PCI interrupt requests from each of the plurality of PCI interrupt sources to one or more of the plurality of interrupt inputs INTA – INTD of the interrupt controller 32.

Therefore, contrary to Applicants' argument, the interrupt sources are the PCI devices 18, 20, 22, and 24. It is clear that interrupt sources generate interrupt requests, or in other words, interrupt requests are originated/generated from interrupt sources. It is also clear from the rejection above that each of the interrupt sources (each of PCI devices 18, 20, 22, and 24) is mapped into each of a plurality of interrupt inputs 52, 54, 56, and 58, inputted to the interrupt controller unit 32. In addition, it is also clear from the above rejection that interrupt requests INTA, INTB, INTC, INTD, INTN are originated/generated from/by each of a plurality of interrupt sources 18, 20, 22, and 24.

Applicants further argued that "Applicants respectfully disagree with the Examiner's characterization that in all cases a logic OR gate can be used to 'selectively' enable an input that is being asserted. The word 'selectively' means

discriminating of or characterized by selection. (see American Heritage College dictionary, 1235 (Robert B. Costello ed., 3rd Edition, Houghton Mifflin Co. 2000). In the Armstrong patent, by merely being asserted, INTA of PCI device 18 will cause INTA 52 to also be asserted. There is no discrimination in the operation of an OR gate. As shown in the table on page 7 of the Office Action, if an interrupt is present at the input to the gate (represented by the logic "1"), it gets passed along to the output of the gate. There is no selectivity whatsoever in the Armstrong patent, merely the pass-through operation of a logic OR gate. "

In response to Applicants' argument, at the outset, it is noted that the 2-input logic OR and its corresponding truth table are exemplary. It is clear from the rejection that there are more than 2 interrupt requests from a plurality of interrupt sources 18, 20, 22, and 24. See definition of OR gate from Wikipedia and Answer.com, cited below.

Contrary to Applicants' argument, it is clear from the rejection, the resulting output of the OR gate depends on the selection of the input combination of the OR-gate. It is also clear from the rejection that the number of interrupt requests INTA, INTB, INTC, INTD, INTN, originated/generated from/by each of a plurality of interrupt sources 18, 20, 22, and 24, is more than the number of the interrupt inputs 52, 54, 56, and 58. Thus, the shared or wired-OR interrupt binding architecture of Armstrong selectively enables interrupt requests INTA, INTB, INTC, INTD, INTN from each of a plurality of interrupt sources 18, 20, 22, and 24 to one or more of the interrupt inputs 52, 54, 56, and 58. Applicants also argued that "there is no discrimination in the operation of the OR gate." Contrary to Applicants' argument, the input combination of

the OR gate is the discriminating factor. In other words, the resulting output of the OR gate depends on the selection of the input combination of the OR-gate. In any event, no discriminating factors or any criteria that the "selection" is based upon is claimed. In fact, claim 1, for example, only requires "selectively enabling interrupt requests from each of the plurality of interrupt sources to one or more of the plurality of interrupt inputs."

The Wach 102 Rejection:

With regard to claims 1-23, Applicants argued that "[a]s disclosed in the Wach patent, the storage locations GF are part of group register 44, which must be read by the processor 14. The Wach patent refers to the storage locations GF as interrupt groups. Basically, each successive pair of interrupt sources forms an interrupt group (see column 6, lines 9-21). The register 44 is associated with one of the interrupt inputs, namely interrupt line 26. When an interrupt is received on this line, the register 44 identifies which group contains the interrupt source that generated the interrupt (column 6, lines 21-24)."

In response to Applicants' argument, at the outset, it is noted that Applicants, instead of pointing out the supposed errors in the Examiner's rejection, choose to interpret the Wach rejection in a different way using portions of Wach's disclosure, taken out of context, for support.

As clearly pointed out in the rejection, which is reproduced below (with emphasis added):

Wach discloses an interrupt architecture employing interrupt sharing, which is best illustrated in the following figure:

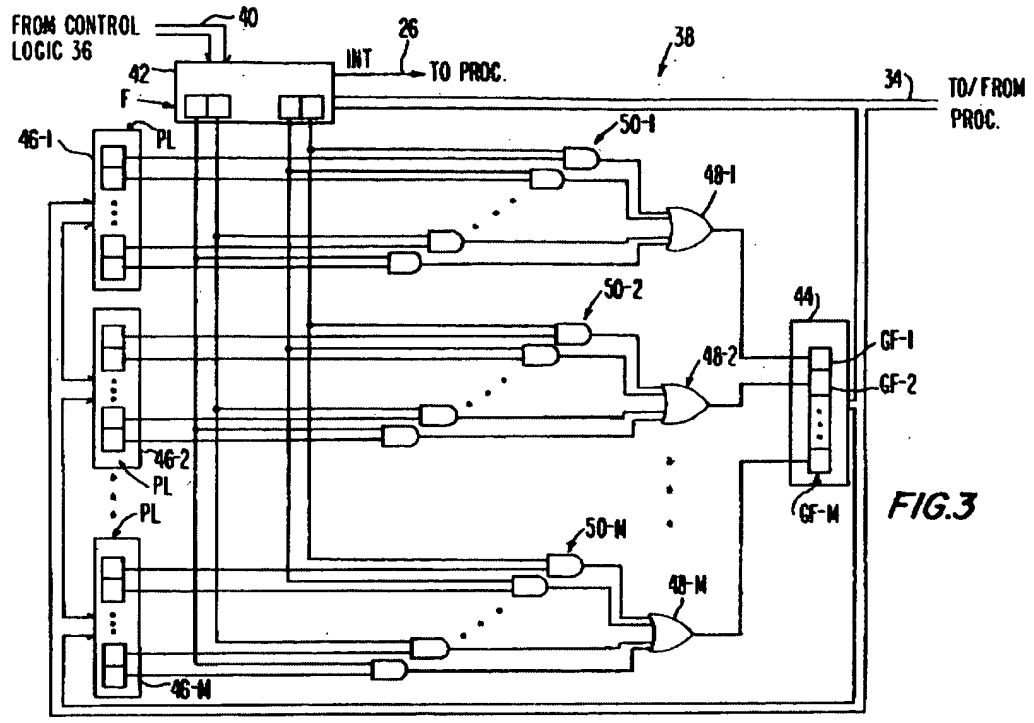

FIG.3

At the outset, **in order to have a clear understanding of the following discussion, it is important to note that the interrupt requests can be generated from register 44 instead of register 42 (see column 11, lines 10-15). In addition, the term "group" used in Wash includes group that has only one interrupt resource (see column 11, lines 47-49).**

As shown above and specifically described in column 4, line 63 to column 6, line 43; column 10, line 55 to column 11, line 48, the number of storage locations F in register 42 is equal to the number of interrupt sources, any one of which may cause the

transmission of the interrupt signal to processor 14. Also, the locations F correspond one-to-one to the interrupt sources. The plurality of interrupt resources are routed or mapped to a plurality of interrupt inputs represented by a plurality of locations GF; wherein the interrupt request signal generated when any one or more of the locations GF are set. Further, in Wash, a masking bit is used to enable or disable interrupt requests from each of a plurality of interrupt sources to one or more of the plurality of interrupt inputs. Specifically, when it is desired to mask a given one of the interrupt sources, processor 14 sends programming signals to the association registers 46 such that the value "0" is stored in the respective location PL corresponding to the interrupt source to be masked.

Applicants further argued that "Applicants respectfully submit that the claimed interrupt inputs are not the same as the plurality of locations GF of register 44 disclosed in the Wach patent. The plurality of locations GF are merely storage locations read by the processor 14 in response to an interrupt request on line 26."

Contrary to Applicants' argument, it is clear that a plurality of location GF of register 44 is readable as a plurality of interrupt inputs. As disclosed in [0012], page 4 of Applicants' originally filed specification and as shown in Fig. 3, the interrupt inputs are defined as follows:

[0012] In yet another aspect of the invention, a system is disclosed for sharing a plurality of interrupt inputs associated with a processor among a plurality of interrupt sources. The system comprises, for each interrupt input, a plurality of logical ANDs, each corresponding to an interrupt source, the corresponding interrupt source providing an interrupt request signal to the corresponding logical AND to interrupt the processor. A plurality of control bits each correspond to an interrupt source and each respectively provide a control bit value to the corresponding logical AND, wherein, based on the control bit value, a corresponding interrupt request signal is provided at an output of the corresponding logical AND. A logical OR is arranged to indicate, to the interrupt input, the presence of a corresponding interrupt request signal from at least one output of the plurality of logical ANDs.

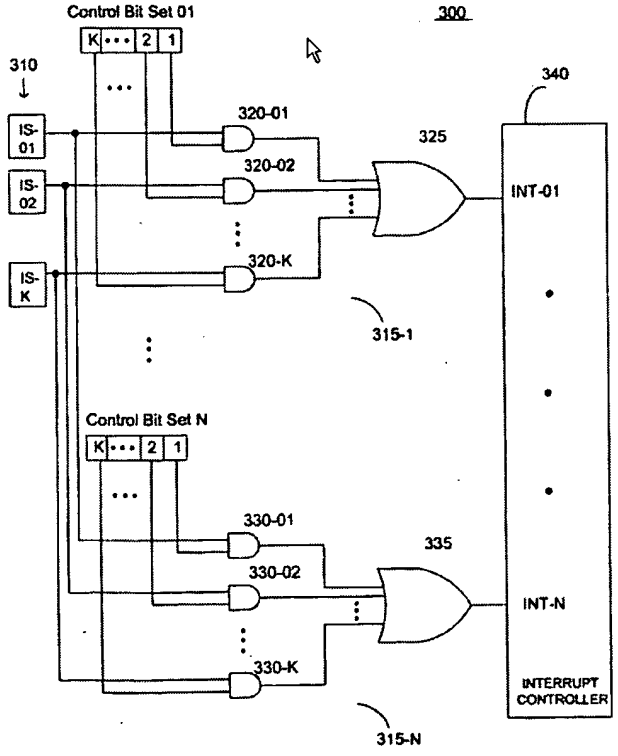

FIG. 3

Identically disclosed and shown in **Fig. 3 of Wach:**

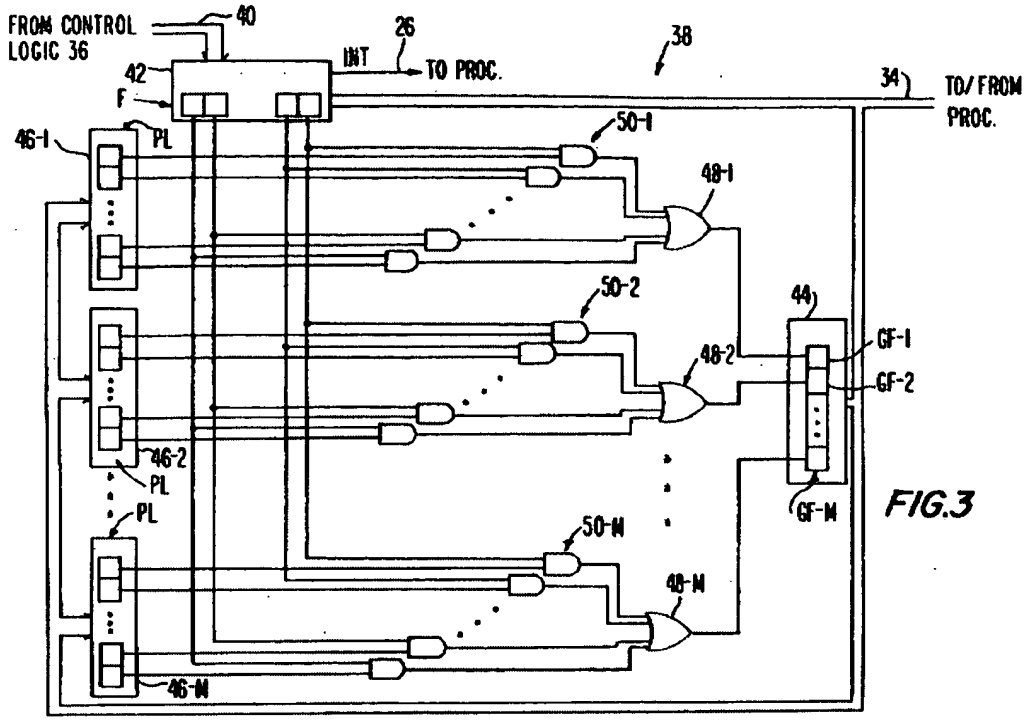

FIG.3

It is clear from at least Fig. 3 of Wach, a logical OR is arranged to indicate, to the location GF or interrupt input, the presence of a corresponding interrupt request signal from at least one output of a plurality of logical AND gates.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Dang whose telephone number is 571-272-3626. The examiner can normally be reached on Monday-Friday from 9:AM to 5:PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart, can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Khanh Dang
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